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WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a PMOS transistor formed in a N-type well;

an NMOS transistor formed in a P-type well;

a plurality of contact holes for connecting a first-layer metal line layer with gate electrodes and diffusion layers of said PMOS and NMOS transistors; and

an electrical conductive layer embedded in said plurality of contact holes, wherein

said plurality of contact holes have at least two types of plane configurations.

2. A semiconductor integrated circuit device as claimed in Claim 1, wherein at least lengths of one sides of said plurality of contact holes existing on said semiconductor integrated circuit device are the same.

3. A semiconductor integrated circuit device as claimed in Claim 1, wherein at least one contacting means for connecting said gate electrodes to said diffusion layers is provided only by electrical conductive layers embedded in said plurality of contact holes.

4. A semiconductor integrated circuit device as claimed in Claim 1, wherein sources or drains of said transistors are wired by using at least said electrical conductive layers embedded in said plurality of contact holes.

5. A semiconductor integrated circuit device as claimed in Claim 1, wherein an area of a contact hole connected to a diffusion layer of a source of said transistor is larger than an area of a contact hole connected to a diffusion layer of a drain of said transistor.

6. A semiconductor integrated circuit device as claimed in Claim 1, wherein said wells are wired by using at least said electrical conductive layers embedded in said plurality of contact holes.

7. A semiconductor integrated circuit device comprising:

a PMOS transistor formed in a N-type well;

an NMOS transistor formed in a P-type well;

first-layer metal line layers;

second-layer metal line layers;

a plurality of contact holes for connecting said first-layer metal line layers to gate electrodes and diffusion layers of said PMOS and NMOS transistors; and

through holes for connecting said first-layer metal line layers to said second-layer metal line layers, wherein

a potential of said N-type well and a potential of said P-type well are controlled independently of each other;

lines for obtaining the potentials of said N-type and P-type wells includes said first-layer metal

line layers, electrical conductors formed inside said contact holes, or said electrical conductors formed inside said contact holes and said first-layer metal line layers; and

said second-layer metal line layers wire a power supply potential and a ground potential.

8. A semiconductor integrated circuit device as claimed in Claim 7, wherein a channel direction of said transistors is parallel to a direction of said lines for controlling said potentials of said N-type P-type wells and to a direction of said lines for said power supply potential and said ground potential.

9. A semiconductor integrated circuit device as claimed in Claim 7, wherein

said electrical conductors formed inside said contact holes and said first-layer metal line layers are formed with tungsten as a main constituent; and

said second-layer metal line layers are formed with copper as a main constituent.

10. A semiconductor integrated circuit device as claimed in Claim 7, wherein said first-layer metal line layers are thinner than said second-layer metal line layers.

11. A semiconductor integrated circuit device as claimed in Claim 7, wherein

said semiconductor integrated circuit device is formed on a P-type substrate; and

said P-type well is formed inside a deep N-

type well formed on said P-type substrate.

12. A semiconductor integrated circuit device as claimed in Claim 9, wherein

a dynamic random access memory is integrated on an identical chip on which said semiconductor integrated circuit device is integrated, said dynamic random access memory using memory cells each of which includes one capacitance element and one transistor; and

bit lines of said dynamic random access memory are formed said first-layer metal line layers.

13. A semiconductor integrated circuit device as claimed in Claim 12, wherein said capacitance element is formed at a height between a height of said first-layer metal line layer and a height of said second-layer metal line layer.

14. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a first line layer formed on said substrate;

a second line layer formed on said first line layer; and

a contact hole for electrically connecting two of a source, gate and drain of said MIS transistor, said first line layer and said second line layer, wherein

when an X-Y plane is assumed on a surface of said substrate, configuration of projection onto said X-Y plane of the source, gate and drain of said transistor, said first line layer or said second line

layer which are connected by said contact hole has a non-overlapped portion.

15. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a first line layer formed on said substrate;

a second line layer formed on said first line layer; and

a contact hole for electrically connecting two of a source, gate and drain of said MOS transistor, said first line layer and said second line layer, wherein

when an X-Y plane is assumed on a surface of said substrate, configuration of projection onto said X-Y plane of a contact portion at which said two of the source, gate and drain of said transistor, said first line layer and said second line layer are connected by said contact hole has a non-overlapped portion.

16. A semiconductor integrated circuit device as claimed in Claim 14 or 15, wherein an electrical conductor is embedded in said contact hole.

17. A semiconductor integrated circuit device as claimed in any one of Claims 14 to 16, wherein said first and second line layers are metal line layers.

18. A semiconductor integrated circuit device, comprising:

a diffusion layer formed in a substrate;

an intermediate layer formed on said substrate;

a line layer formed on said intermediate layer; and

a contact hole formed within said intermediate layer for electrically connecting said diffusion layer to said line layer, wherein

when an X-Y plane is assumed on a surface of said substrate, configuration of projection onto said X-Y plane of a contact portion of said diffusion layer and said contact hole and configuration of projection onto said X-Y plane of a contact portion of said line layer and said contact hole have non-overlapped portions.

19. A semiconductor integrated circuit device, comprising:

a first line layer formed on a substrate;

an intermediate layer formed on said first line layer;

a second line layer formed on said intermediate layer; and

a contact hole formed within said intermediate layer for electrically connecting said first line layer to said second line layer, wherein

when an X-Y plane is assumed on a surface of said substrate, configuration of projection onto said X-Y plane of a contact portion of said first line layer to said contact hole and configuration of projection onto said X-Y plane of a contact portion of said second line layer and said contact hole have non-overlapped portions.

20. A semiconductor integrated circuit device as claimed in Claim 19, wherein

an electrical conductor formed inside said contact hole and said first-layer metal line layer are formed of a metal which contains tungsten as a main constituent; and

said second-layer metal line layer is formed of a metal which contains copper as a main constituent.

21. A semiconductor integrated circuit device as claimed in Claim 19 or 20, wherein said first-layer metal line layer is thinner than said second-layer metal line layer.

22. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a first metal line layer formed on said substrate; and

a second metal line layer formed on said first metal line layer, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second metal line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first metal line layer; and

at least a part of said power supply line and said well potential line is overlapped.

23. A semiconductor integrated circuit device as claimed in Claim 22, wherein said power supply line completely overlaps with said well potential line.

24. A semiconductor integrated circuit device as claimed in Claim 22 or 23, wherein a width of said power supply line is greater than a width of said well potential line.

25. A semiconductor integrated circuit device as claimed in any one of Claims 22 to 24, wherein

said first metal line layer is formed of a metal a main constituent of which is tungsten; and

said second metal line layer is formed of a metal a main constituent of which is copper.

26. A semiconductor integrated circuit device as claimed in any one of Claims 22 to 25, wherein said first metal line layer is thinner than said second metal line layer.

27. A semiconductor integrated circuit device as claimed in any one of Claims 22 to 26, wherein

a contact hole is formed in an intermediate layer between said substrate and said first metal line layer;

said contact hole overlaps with said first metal line which constitutes said part of said well potential line; and

said contact hole constitutes said part of said well potential line.

28. A semiconductor integrated circuit device,

comprising:

a MIS transistor formed in a substrate;

a first metal line layer formed on said substrate;

an intermediate layer formed between said substrate and said first metal line layer; and

a second metal line layer formed on said first metal line layer, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second metal line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by an electrical conductor which is formed inside a contact hole formed within said intermediate layer; and

said power supply line overlaps with said contact hole.

29. A semiconductor integrated circuit device as claimed in Claim 28, wherein a width of said power supply line is greater than a width of said contact hole.

30. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a first metal line layer formed on said substrate; and

a second metal line layer formed on said first metal line layer, wherein

at least a part of a power supply line connected to a source/drain channel in said MOS transistor is constituted by said second metal line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first metal line layer; and

said first metal line layer is formed of tungsten as a main constituent; and

said second metal line layer is formed of copper as a main constituent.

31. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a memory cell for storing data;

a first metal line layer formed on said substrate; and

a second metal line layer formed on said first metal line layer, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second metal line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first metal line layer; and

at least a part of a bit line for transmitting an input or output data signal to said memory cell is constituted by said first metal line layer.

32. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a memory cell for storing data;

a first line layer a main constituent of which is tungsten; and

a second line layer a main constituent of which is copper, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second line layer;

at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first line layer; and

at least a part of a bit line for transmitting an input or output data signal to said memory cell is constituted by said first line layer.

33. A semiconductor integrated circuit device, comprising:

a MIS transistor formed in a substrate;

a memory cell for storing data;

a first metal line layer formed on said substrate, a main constituent of said first metal line layer being tungsten; and

a second metal line layer formed on said first

metal line layer, a main constituent of said second metal line being copper, wherein

at least a part of a power supply line connected to a source/drain channel in said MIS transistor is constituted by said second metal line layer; and

at least a part of a bit line for transmitting an input or output data signal to said memory cell is constituted by said first metal line layer.

34. A semiconductor integrated circuit device as claimed in Claim 33, wherein at least a part of a well potential line for controlling a well potential of said MIS transistor is constituted by said first metal line layer.

35. A semiconductor integrated circuit device as claimed in Claim 33 or 34, wherein

said memory cell is a DRAM cell; and

a capacitor of said DRAM cell is located between said first metal line layer and said second metal line layer.

36. A semiconductor integrated circuit device as claimed in any one of Claims 33 to 35, wherein a gate electrode layer is located between said substrate and said first metal line layer.

37. A semiconductor integrated circuit device as claimed in any one of Claims 33 to 36, further comprising:

a contact hole for connecting two of said

substrate, said first metal line layer, said second metal line layer and said gate electrode layer which are selected as a first connection object and a second connection object, wherein

when an X-Y plane is assumed on a surface of said substrate, projection onto said X-Y plane of a contact surface of said first connection object and said contact hole has a portion at which said projection does not overlap with a mapping onto said X-Y plane of a contact surface of said second connection object and said contact.